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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3
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**Complete if Known**

Application Number	09/312,302
Filing Date	05/14/1999
First Named Inventor	Mario Nemirovsky
Art Unit	2154
Examiner Name	Larry Donaghue
Attorney Docket Number	P3803

## U. S. PATENT DOCUMENTS

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## FOREIGN PATENT DOCUMENTS

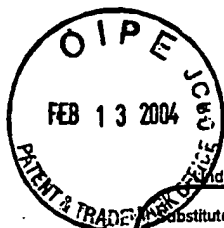
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Examiner Signature	Date Considered	09/29/05
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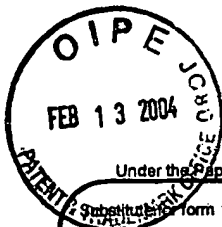
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Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
		MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
		POTEL, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp. 72-77, San Jose, CA	
		ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
		ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at : <a href="http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS">http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS</a> )	
		MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp. 10-66, 10-67 and 10-71, Motorola, Inc.	
		DIEFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp.40-63, Vol. 12, No. 2	
		KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp 7-106 and 7-107, Prentice Hall, New Jersey	
		DIEFENDORFF, KEITH et al., AltiVec Extension to PowerPC Accelerates Media Processing, March - April 2000, pp. 85-95, IEEE Micro, Vol. 20, No. 2	
		PAI, VIJAY et al., An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors, Proceedings of ASPLOS-VII, October 1996, pp. 12-23, ACM, Inc.,	

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Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
g		GRUNEWALD, WINFRIED et al., Towards Extremely Fast Context Switching in a Block-Multithreaded Processor, Proceedings of EUROMICRO-22, 1996, pp. 592-599	
es		BRADFORD, JEFFREY et al., Efficient Synchronization for Multithreaded Processors, Workshop on Multithreaded Execution, Architecture and Compilation, January-February 1998, pp. 1-4	
sp		TULLSEN, DEAN et al., Supporting Fine-Grained Synchronization on a Simultaneous Multithreading Processor, UCSD CSE Technical Report CS98-587, June 1998, all pages, US	

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